REMARKS

In the Office Action, the Examiner noted that claims 1-8 and 12-16 are pending in the application and that claims 1-8 and 12-16 are rejected. By this response, claims 1-8 and 12-16 continue without amendment. In view of the following discussion, the Applicant submits that none of the claims now pending in the application are indefinite under the provisions of 35 U.S.C. §112, anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Thus, the Applicant believes that all of these claims are now in condition for allowance.

I. Objections

The Examiner objected to the drawings as not showing every feature of the invention specified in the claims. In particular, the Examiner stated that the drawings do not show an integrated circuit package having an array of landing pads disposed on an inside surface thereof in a second pattern and an array of solder balls disposed on an outside surface of the integrated circuit package. (Office Action, p. 2). The Applicant respectfully disagrees.

FIG. 10 shows an integrated circuit package (1012) having an array of landing pads disposed on an inside surface thereof (1014) in a pattern. An array of solder balls (1023) is disposed on an outside surface of the integrated circuit package (1012). See also Applicant's specification, paragraphs 0089 through 0091. Thus, FIG. 10 clearly shows the features cited by the Examiner. No new drawings or amendments to the drawings are required. Accordingly, the Applicant respectfully requests that the objection to the drawings be withdrawn.

II. Rejection of Claims under 35 U.S.C. §112

The Examiner rejected claims 1-8 and 12-16 as being indefinite. In particular, the Examiner stated that the features "'an integrated circuit package having an array of landing pads disposed on an inside surface of the integrated circuit package in a second pattern and array of solder balls disposed on an outside surface of the integrated circuit package" is unclear and confusing.'" (Office Action, p. 3). The Applicant respectfully disagrees.

As described above, Applicant's FIG. 10 shows an integrated circuit package having an array of landing pads disposed on an inside surface thereof in a pattern. This is also described in paragraph 0089 of Applicant's specification. Moreover, this feature is clear on its face as understood by one skilled in the art. That is, an integrated circuit package clearly has an inside surface and an array of landing pads may be formed on such inside surface. In addition, Applicant's FIG. 10 shows an array of solder balls disposed on an outside surface thereof. This is also described in paragraph 0091 of Applicant's specification. Moreover, this feature is clear on its face as understood by one skilled in the art. That is, an integrated circuit package clearly has an outside surface opposite the inside surface and an array of solder balls may be formed on such outside surface.

Furthermore, the aforementioned features are also clear within the context of the claims. An interposing structure is disposed inside the integrated circuit package between the integrated circuit die and the inside surface of the integrated circuit package. Also, the array of landing pads disposed on the inside surface of the integrated circuit package are in a substantially identical pattern as micro-bumps disposed on the integrated circuit die. Again, these features are clearly shown in FIG. 10, as well as being clear on their face.

Finally, the Examiner did not set forth a specific rationale as to why the cited features are unclear or confusing. The Applicant contends that such features recited in claims 1 and 12 are clear and definite, as set forth above.

Claims 2-8 and 13-16 depend from claims 1 and 12 and were rejected as being dependent upon claims 1 and 12. Since claims 1 and 12 are definite, claims 2-8 and 13-16 are also definite. Therefore, the Applicant contends that claims 1-8 and 12-16 are definite and, as such, fully comply with 35 U.S.C. §112, second paragraph. Accordingly, the Applicant respectfully requests that the present rejection be withdrawn.

III. Rejection of Claims under 35 U.S.C. §102

The Examiner rejected claims 1-7, 12, and 14-15 as being anticipated by Chakravorty (U.S. Patent 6,970,362, issued November 29, 2005). The rejection is respectfully traversed.

More specifically, the Examiner stated that Chakravorty teaches an integrated circuit package having an array of landing pads disposed on an inside surface of the package and an array of solder balls disposed on an outside surface of the package. (Office Action, p. 4). The Applicant respectfully disagrees.

Chakravorty teaches a die (40) coupled to a primary substrate (60) using an interposer (50). (Chakravorty, FIG. 2). The interposer includes landing pads (44) coupled to bumps (42) of the die, and landing pads (56) coupled to bumps (58) of the primary substrate. (Chakravorty, FIG. 2). The bumps of the primary substrate are coupled to landing pads (61-67) on a surface thereof. Embodiments shown in FIGs. 3-5 of Chakravorty are similar to that of FIG. 2.

Chakravorty, however, does not teach or suggest each and every element of Applicant's claim 1. Namely, Chakravorty does not teach or suggest an array of solder balls disposed on the outside surface of the integrated circuit package. Chakravorty shows only two sets of bumps or solder balls, namely, the bumps (42) on the die and the bumps (58) of the primary substrate. Neither of these bumps, however, teach or suggest the solder balls recited in Applicant's claim 1.

Notably, the bumps (42) are disposed on the die in Chakravorty and not an outside surface of the integrated circuit package. The bumps (58) of the primary substrate in Chakravorty are disposed on the inside surface thereof, not the outside surface. In particular, the Examiner cited the landing pads (61-67) on the primary substrate as being an "array of landing pads disposed on an inside surface of the integrated circuit package." (Office Action, p. 4). Since these landing pads are coupled to the bumps (58), the bumps (58) of Chakravorty are on the inside of the substrate, not the outside. In essence, Chakravorty does not teach or suggest an integrated circuit package, as recited in Applicant's invention. Rather, Chakravorty shows an integrated circuit die coupled to a substrate, such as a circuit board, using an interposer.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984). Since Chakravorty does not teach an array of solder balls disposed on the outside surface of the integrated circuit package, Chakravorty does not teach each and every element of Applicant's claim 1 as arranged therein. Accordingly, Chakravorty does not anticipate Applicant's invention recited in claim 1.

Claim 12 is includes features similar to those of claim 1 emphasized above. For the same reasons set forth above, the Applicant contends that Chakravorty does not anticipate the invention of claim 12. Claims 2-7 and 14-15 depend, either directly or indirectly, from claims 1 and 12 and recite additional features therefor. Since Chakravorty does not anticipate Applicant's invention as recited in claims 1 and 12, dependent claims 2-7 and 14-15 are also not anticipated and are allowable. Therefore, the Applicant contends that claims 1-7, 12, and 14-15 are not anticipated by Chakravorty and, as such, fully satisfy the requirements of 35 U.S.C. §102. The Applicant respectfully requests that the present rejection be withdrawn.

II. Rejection Of Claims Under 35 U.S.C. §103

A. Claim 16

The Examiner rejected claim 16 as being unpatentable over Chakravorty in view of Berlin (U.S. Patent 6,104,082, issued August 15, 2000). The rejection is respectfully traversed.

Claim 16 depends from claim 12 and recites additional features therefor. The cited references, either singly or in any permissible combination, do not teach, suggest, or otherwise render obvious Applicant's invention recited in claim 12. Namely, the cited combination does not teach or suggest an array of solder balls disposed on the outside surface of the integrated circuit package. As described above, Chakravorty is devoid of such a teaching. Berlin teaches a structure similar to that of Chakravorty. (See Berlin, FIGs. 2B, 2C). That is, Berlin shows chips coupled to an interposer (60), which is in turn coupled to a substrate (68). (Berlin, FIG. 2B). While Berlin shows bumps (62) that couple the chips to the interposer, and bumps (69)

that couple the interposer to the substrate (68), Berlin is devoid of any teaching or suggestion of solder balls on the outside surface of the substrate (68). Like Chakravorty, Berlin does not teach or suggest an integrated circuit package, but rather a structure for coupling chips to a substrate, such as a PCB. Since neither Chakravorty nor Berlin teach or suggest an array of solder balls disposed on the outside surface of the integrated circuit package, no conceivable combination of Chakravorty and Berlin renders obvious Applicant's invention of claim 12. Therefore, Applicants contend that claim 16, which depends from claim 12, is patentable over Chakravorty and Berlin and fully satisfies the requirements of 35 U.S.C. §103.

B. Claims 7 and 13

The Examiner rejected claims 7 and 13 as being unpatentable over Chakravorty in view of Vafi (U.S. Patent 5,474,458, issued December 12, 1995). The rejection is respectfully traversed.

Claims 7 and 13 depend from claims 1 and 12 and recite additional features therefor. The cited references, either singly or in any permissible combination, do not teach, suggest, or otherwise render obvious Applicant's invention recited in claims 1 and 12. Namely, the cited combination does not teach or suggest an array of solder balls disposed on the outside surface of the integrated circuit package. As described above, Chakravorty is devoid of such a teaching. Vafi generally teaches an interconnect carrier for coupling integrated circuit chips to substrates. Vafi teaches a structure similar to both Chakravorty and Berlin. That is, Vafi shows a chip (1) coupled to an interconnect carrier (10), which is in turn coupled to a substrate (3). (Vafi, FIG. 3). While Vafi shows bumps (15) that couple the chip to the interconnect carrier, and bumps (15) that couple the interposer to the substrate (68), Vafi is devoid of any teaching or suggestion of solder balls on the outside surface of the substrate (3). Like Chakravorty and Berlin, Vafi does not teach or suggest an integrated circuit package, but rather a structure for coupling a chip to a substrate, such as a PCB. Since neither Chakravorty nor Vafi teach or suggest an array of solder balls disposed on the outside surface of the integrated circuit package, no conceivable combination of Chakravorty and Vafi renders obvious Applicant's invention of claims 1 and 12. Therefore,

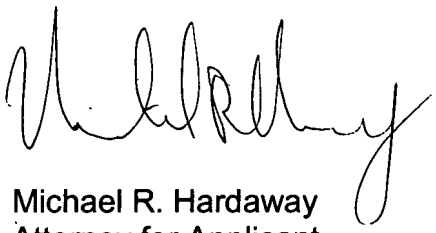
Applicants contend that claims 7 and 13, which depend from claims 1 and 12, are patentable over Chakravorty and Vafi and fully satisfy the requirements of 35 U.S.C. §103.

CONCLUSION

Thus, Applicant submits that none of the claims presently in the application are indefinite under the provisions of 35 U.S.C. §112, anticipated under the provisions of 35 U.S.C. §102, or obvious under the provisions of 35 U.S.C. §103. Consequently, Applicant believes that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Applicant's Attorney at (408) 879-6149 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,



Michael R. Hardaway
Attorney for Applicant
Reg. No. 51,992

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on April 6, 2007.

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